What is claimed is :

1. Alignment marks comprising: a wafer, first alignment marks formed over the wafer, and second alignment marks covering the first alignment marks, wherein

the second alignment marks allow an alignment beam to permeate and the first alignment marks reflect the alignment beam, whereby serving as an alignment reference for the following step.

2. The alignment marks as set forth in Claim 1, wherein the alignment beam is a laser beam and the second alignment marks are formed of a red filter.

3. The alignment marks as set forth in Claim 1, wherein the second alignment marks are formed to be 1μm or more in thickness.

4. Alignment marks comprising: a wafer, first alignment marks formed over the wafer, and third alignment marks provided in the vicinity of the first alignment marks, wherein

the third alignment marks are formed based on the first alignment marks as a reference, the alignment beam is diffracted at a step portion formed by the third alignment marks, and whereby the third alignment marks serve as an alignment reference for the following step.

5. The alignment marks as set forth in Claim 4, wherein the alignment beam is a laser beam, the third alignment marks are formed of a red filter.

6. The alignment marks as set forth in Claim 4, wherein the third alignment marks are formed to be 1μm or

more in thickness.

7. The alignment marks as set forth in Claim 1, wherein the first alignment marks are made of the same materials as those of the source and drain electrodes of a thin-film transistor and provided on the same base film as a base film of the source and drain electrodes.

8. The alignment marks as set forth in Claim 4, wherein the first alignment marks are made of the same materials as those of the source and drain electrodes of a thin-film transistor and provided on the same base film as a base film of the source and drain electrodes.

9. Alignment marks comprising: a wafer, fourth alignment marks formed over the wafer, and fifth alignment marks provided on the fourth alignment marks, wherein

the total thickness of the fourth alignment marks and the fifth alignment marks are formed to be 0.5μm or more in thickness.

10. The alignment marks as set forth in Claim 9, wherein the fourth alignment marks comprise a semiconductor layer which is made of the same materials as those of a semiconductor layer of a thin-film transistor and provided on the same base film as a base film of the semiconductor layer, and the fifth alignment marks are made of the same materials as those of the source and drain electrodes of the thin-film transistor.

11. A manufacturing method for alignment marks comprising the steps of:

forming a thin-film transistor including at least a

gate electrode, a gate insulating film, a semiconductor thin film, source and drain electrodes on a wafer;

forming alignment reference marks by using the same materials as those of at least one of the gate electrode, the semiconductor film, and the source and drain electrodes in an area other than a formation area for the thin-film transistor at the same time when the gate electrode, the semiconductor film and the source and drain electrodes are formed:

forming red filter alignment reference marks comprising a red filter so as to cover the alignment reference marks; and

then, performing alignment of the following step pattern based on the alignment reference marks below the red filter alignment marks.

12. The manufacturing method for alignment marks as set forth in Claim 11, wherein

the alignment reference marks are formed at the same time as source and drain electrodes with a shading property are formed, and alignment is performed by means of light reflection caused by the alignment reference marks.

13. A manufacturing method for alignment marks comprises the steps of:

forming a thin-film transistor including at least a gate electrode, a gate insulating film, a semiconductor thin film, source and drain electrodes on a wafer;

forming alignment reference marks by using the same materials as those of at least one of the gate electrode,

the semiconductor film, and the source and drain electrodes in an area other than a formation area for the thin-film transistor, at the same time as the gate electrode, the semiconductor film, and the source and drain electrodes are formed;

forming a red filter alignment reference marks comprising a red filter in the area other than the thin-film transistor formation area and distant from the alignment reference marks with the alignment reference marks as a reference; and

then, performing alignment of the following step pattern with the red filter alignment reference marks as a reference.

14. The manufacturing method for alignment marks as set forth in Claim 13, wherein alignment is performed by diffracted light at a step portion formed by the red filter alignment reference marks.

15. A manufacturing method for alignment marks comprised the steps of:

forming a thin-film transistor including at least a gate electrode, a gate insulating film, a semiconductor thin film, source and drain electrodes on a wafer;

forming alignment reference marks having a laminated structure comprising the semiconductor thin film and the source and drain electrodes by using the same materials as those of the semiconductor film and the source and drain electrodes composing the thin-film transistor; and then,

performing alignment of the following step pattern

with the laminated structure alignment reference marks as a reference.

16. The manufacturing method for alignment marks as set forth in Claim 15, wherein the semiconductor film comprises an active semiconductor film as its lower layer and an ohmic semiconductor film as its upper layer

17. The manufacturing method for alignment marks as set forth in Claim 15, wherein alignment is performed by diffracted light at a step portion formed by the laminated structure alignment reference marks.